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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/823,276	03/29/2001	Ryo Inoue	10559-393001/P10258-AD1-	7293
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FISH & RICHARDSON, PC P.O. BOX 1022 MINNEAPOLIS, MN 55440-1022			EXAMINER LI, AIMEE J	
			ART UNIT	PAPER NUMBER
			2183	

DATE MAILED: 01/12/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/823,276	Applicant(s) INOUE ET AL.	
	Examiner Aimee J. Li	Art Unit 2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 26 September 2005.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-21 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-21 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

1. Claims 1-21 have been considered. Claims 1, 3, 7, and 15 have been amended as per Applicant's request.

Papers Submitted

2. It is hereby acknowledged that the following papers have been received and placed of record in the file: RCE as received on 26 September 2005 and Amendment as received on 26 September 2005.

Non-Compliant Amendment Warning

3. Examiner notes that claim 15 is currently identified as "previously presented", however, there are amendments made to the claim. The claim should be identified as "currently amended". In the future, such errors will result in a Notice of Non-Compliant Amendment.

Claim Objections

4. Claim 15 is objected to because of the following informalities: Please correct line 5 from "restore at two or more of the registers" to read --restore [[at]]two or more of the registers--. Appropriate correction is required.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

6. Claims 1-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Thomas, Jr., U.S. Patent Number 5,535,346 (herein referred to as Thomas).

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7. Referring to claim 1, Thomas has taught a method comprising in a processor which has a future file (Thomas Abstract, lines 6-9; column 1, line 54 to column 2, line 4; column 2, lines 12-19 and 23-51; column 4, lines 51-58; column 7, lines 9-49; column 8, lines 14-27; column 8, line 53 to column 9, line 20; Figure 3, Figure 5; Figure 6; and Figure 7) and which is capable of restoring two or more registers of the future file in a single clock cycle (Thomas Abstract, lines 6-9; column 1, line 54 to column 2, line 4; column 2, lines 12-19 and 23-51; column 4, lines 51-58; column 7, lines 9-49; column 8, lines 14-27; column 8, line 53 to column 9, line 20; Figure 3, Figure 5; Figure 6; and Figure 7). Thomas has not explicitly taught restoring two or more registers of the future file over more than one clock cycle when a termination occurs in the processor. However, Thomas has disclosed in column 2, lines 12-19 a future file that “requires numerous cycles to correct its data in the event of an exception” but has a faster lookup for operand data and a future file that “requires only one cycle to correct the data stored in the future file in the event of an exception” but has a slower lookup for operand data. This would have suggested to a person of ordinary skill in the art to create a future file that incorporates both advantages. Then the device would benefit from both advantages dependent on the condition of the system. The future file would have faster exception handling and slower look-ups for data operands when there is a higher chance of an exception and fewer look-ups, but would have faster look-ups for data operands and slower exception handling when there is more look-ups and lower chance of an exception.

8. Referring to claim 2, Thomas has taught wherein the processor is a pipelined processor (Thomas Abstract, lines 6-9; column 1, line 54 to column 2, line 4; column 2, lines 12-19 and 23-

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51; column 4, lines 51-58; column 7, lines 9-49; column 8, lines 14-27; column 8, line 53 to column 9, line 20; Figure 3, Figure 5; Figure 6; and Figure 7).

9. Referring to claim 3, Thomas has taught wherein restoring two or more registers of the future file comprises updating two or more speculative registers in the future file with architectural values (Thomas Abstract, lines 6-9; column 1, line 54 to column 2, line 4; column 2, lines 12-19 and 23-51; column 4, lines 51-58; column 7, lines 9-49; column 8, lines 14-27; column 8, line 53 to column 9, line 20; Figure 3, Figure 5; Figure 6; and Figure 7).

10. Referring to claim 7, Thomas has taught an apparatus comprising:

- a. A control unit coupled to a first set of registers, a second set of registers and a pipeline (Thomas Abstract, lines 6-9; column 1, line 54 to column 2, line 4; column 2, lines 12-19 and 23-51; column 4, lines 51-58; column 7, lines 9-49; column 8, lines 14-27; column 8, line 53 to column 9, line 20; Figure 3, Figure 5; Figure 6; and Figure 7),
- b. The control unit adapted to restoring two or more registers of the first set of registers with data contained in the second set of registers in one clock cycle (Thomas Abstract, lines 6-9; column 1, line 54 to column 2, line 4; column 2, lines 12-19 and 23-51; column 4, lines 51-58; column 7, lines 9-49; column 8, lines 14-27; column 8, line 53 to column 9, line 20; Figure 3, Figure 5; Figure 6; and Figure 7).

11. Thomas has not explicitly taught restore two or more registers of the first set of registers with data contained in the second set of registers over more than one clock cycle following a termination of an instruction in the pipeline. However, Thomas has disclosed in column 2, lines

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12-19 a future file that “requires numerous cycles to correct its data in the event of an exception” but has a faster lookup for operand data and a future file that “requires only one cycle to correct the data stored in the future file in the event of an exception” but has a slower lookup for operand data. This would have suggested to a person of ordinary skill in the art to create a future file that incorporates both advantages. Then the device would benefit from both advantages dependent on the condition of the system. The future file would have faster exception handling and slower look-ups for data operands when there is a higher chance of an exception and fewer look-ups, but would have faster look-ups for data operands and slower exception handling when there is more look-ups and lower chance of an exception.

12. Referring to claim 8, Thomas has taught wherein each register in the second set of registers is associated respectively with a register in the first set of registers (Thomas Abstract, lines 6-9; column 1, line 54 to column 2, line 4; column 2, lines 12-19 and 23-51; column 4, lines 51-58; column 7, lines 9-49; column 8, lines 14-27; column 8, line 53 to column 9, line 20; Figure 3, Figure 5; Figure 6; and Figure 7).

13. Referring to claim 15, Thomas has taught a system comprising:

- a. A static random access memory device (Thomas column 3, lines 14-28; column 4, lines 51-58; and Figure 1);
- b. A processor coupled to the static random access memory device (Thomas column 3, lines 14-28; column 4, lines 51-58; and Figure 1), wherein the processor includes a first set of registers, a second set of registers, a pipeline (Thomas Abstract, lines 6-9; column 1, line 54 to column 2, line 4; column 2, lines 12-19 and 23-51; column 4, lines 51-58; column 7, lines 9-49; column 8, lines 14-27;

column 8, line 53 to column 9, line 20; Figure 3, Figure 5; Figure 6; and Figure 7) and a control unit adapted to restoring the first set of registers with values in the second set of registers in one clock cycle (Thomas Abstract, lines 6-9; column 1, line 54 to column 2, line 4; column 2, lines 12-19 and 23-51; column 4, lines 51-58; column 7, lines 9-49; column 8, lines 14-27; column 8, line 53 to column 9, line 20; Figure 3, Figure 5; Figure 6; and Figure 7).

14. Thomas has not explicitly taught restore two or more of the registers in the first set of registers with values in the second set of registers over more than one clock cycle if a termination occurs in the pipeline. However, Thomas has disclosed in column 2, lines 12-19 a future file that “requires numerous cycles to correct its data in the event of an exception” but has a faster lookup for operand data and a future file that “requires only one cycle to correct the data stored in the future file in the event of an exception” but has a slower lookup for operand data. This would have suggested to a person of ordinary skill in the art to create a future file that incorporates both advantages. Then the device would benefit from both advantages dependent on the condition of the system. The future file would have faster exception handling and slower look-ups for data operands when there is a higher chance of an exception and fewer look-ups, but would have faster look-ups for data operands and slower exception handling when there is more look-ups and lower chance of an exception.

15. Referring to claims 4, 9, and 16, Thomas has taught wherein more than one clock cycle comprises two clock cycles (Thomas Abstract, lines 6-9; column 1, line 54 to column 2, line 4; column 2, lines 12-19 and 23-51; column 4, lines 51-58; column 7, lines 9-49; column 8, lines 14-27; column 8, line 53 to column 9, line 20; Figure 3, Figure 5; Figure 6; and Figure 7).

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16. Referring to claims 5, 10, and 17, Thomas has taught wherein more than one clock cycle comprises three clock cycles (Thomas Abstract, lines 6-9; column 1, line 54 to column 2, line 4; column 2, lines 12-19 and 23-51; column 4, lines 51-58; column 7, lines 9-49; column 8, lines 14-27; column 8, line 53 to column 9, line 20; Figure 3, Figure 5; Figure 6; and Figure 7).

17. Referring to claims 6, 12, and 19, Thomas has taught wherein the processor is a pipelined processor and more than one clock cycle comprises a number of clock cycles required to flush the processor (Thomas Abstract, lines 6-9; column 1, line 54 to column 2, line 4; column 2, lines 12-19 and 23-51; column 4, lines 51-58; column 7, lines 9-49; column 8, lines 14-27; column 8, line 53 to column 9, line 20; Figure 3, Figure 5; Figure 6; and Figure 7). In regards to Thomas, in order for the restoring of the future file due to a misprediction to be effective, the pipeline must be flushed as well.

18. Referring to claims 11 and 18, Thomas has taught wherein the control unit is further adapted to flush the pipeline following the termination of the instruction in the pipeline (Thomas Abstract, lines 6-9; column 1, line 54 to column 2, line 4; column 2, lines 12-19 and 23-51; column 4, lines 51-58; column 7, lines 9-49; column 8, lines 14-27; column 8, line 53 to column 9, line 20; Figure 3, Figure 5; Figure 6; and Figure 7). In regards to Thomas, in order for the restoring of the future file due to a misprediction to be effective, the pipeline must be flushed as well.

19. Referring to claims 13 and 20, Thomas has taught the control unit further adapted to restore at least one register in the first set of registers after the pipeline has been flushed (Thomas Abstract, lines 6-9; column 1, line 54 to column 2, line 4; column 2, lines 12-19 and 23-51; column 4, lines 51-58; column 7, lines 9-49; column 8, lines 14-27; column 8, line 53 to column

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9, line 20; Figure 3, Figure 5; Figure 6; and Figure 7). In regards to Thomas, in order for the restoring of the future file due to a misprediction to be effective, the pipeline must be flushed as well.

20. Referring to claims 14 and 21, Thomas has taught wherein the pipeline is an X-stage pipeline, the control unit adapted to restore the first set of registers with data contained in the second set of registers over X-N clock cycles or fewer, following a termination of an instruction in an Nth stage of the pipeline (Thomas Abstract, lines 6-9; column 1, line 54 to column 2, line 4; column 2, lines 12-19 and 23-51; column 4, lines 51-58; column 7, lines 9-49; column 8, lines 14-27; column 8, line 53 to column 9, line 20; Figure 3, Figure 5; Figure 6; and Figure 7).

Response to Arguments

21. Applicant's arguments with respect to claims 1-21 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

22. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure as follows. Applicant is reminded that in amending in response to a rejection of claims, the patentable novelty must be clearly shown in view of the state of the art disclosed by the references cited and the objections made. Applicant must also show how the amendments avoid such references and objections. See 37 CFR § 1.111(c).

- a. Yeager et al., U.S. Patent Number 5,758,112, has taught a register renaming system that restores the register renaming tables in one clock cycle.
- b. Tran et al., U.S. Patent Number 6,112,018, has taught a system that restores the future file.

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c. Jun et al., U.S. Patent Number 6,112,310, has taught slowing the clock frequency to conserve power.

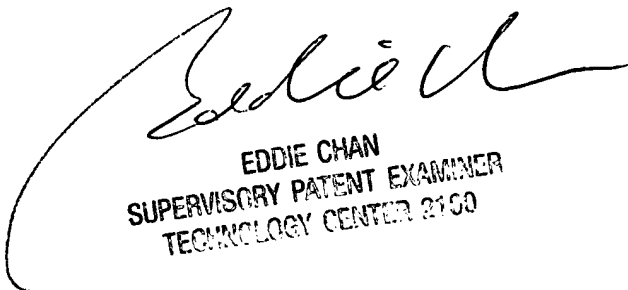
d. Anderson et al., U.S. Patent Number 6,898,695, has taught restoring a future file.

23. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aimee J. Li whose telephone number is (571) 272-4169. The examiner can normally be reached on M-T 7:30am-5:00pm.

24. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

25. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

AJL
Aimee J. Li
4 January 2006



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